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GB 2169173 A GB 2155720 A GB 1543910 A
EP 0309346 A1 US 4602127 A

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(54) Automatic vehicle recognition and service data transmission system

(57) An automatic vehicle recognition system comprises a transmitter 3 attached to a vehicle and a receiver at a vehicle station for receiving information transmitted by the transmitter. A loop 1 embedded in the ground at the station is connected to the receiver and the system is powered up by the presence of the vehicle when the vehicle wheels 2 are within the loop. Information is then transmitted by the transmitter 3 to the receiver and manipulated to provide information about fuel consumption, mileage, vehicle identification and other relevant data.

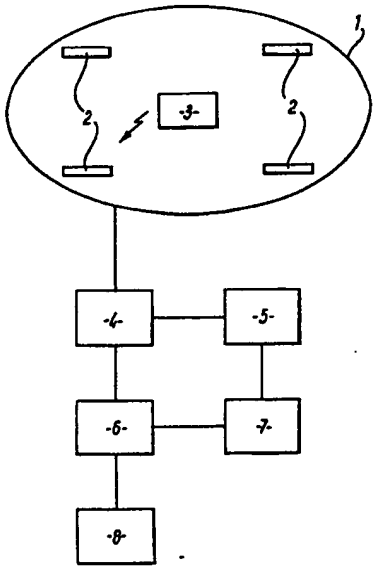

Fig 1

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1982.

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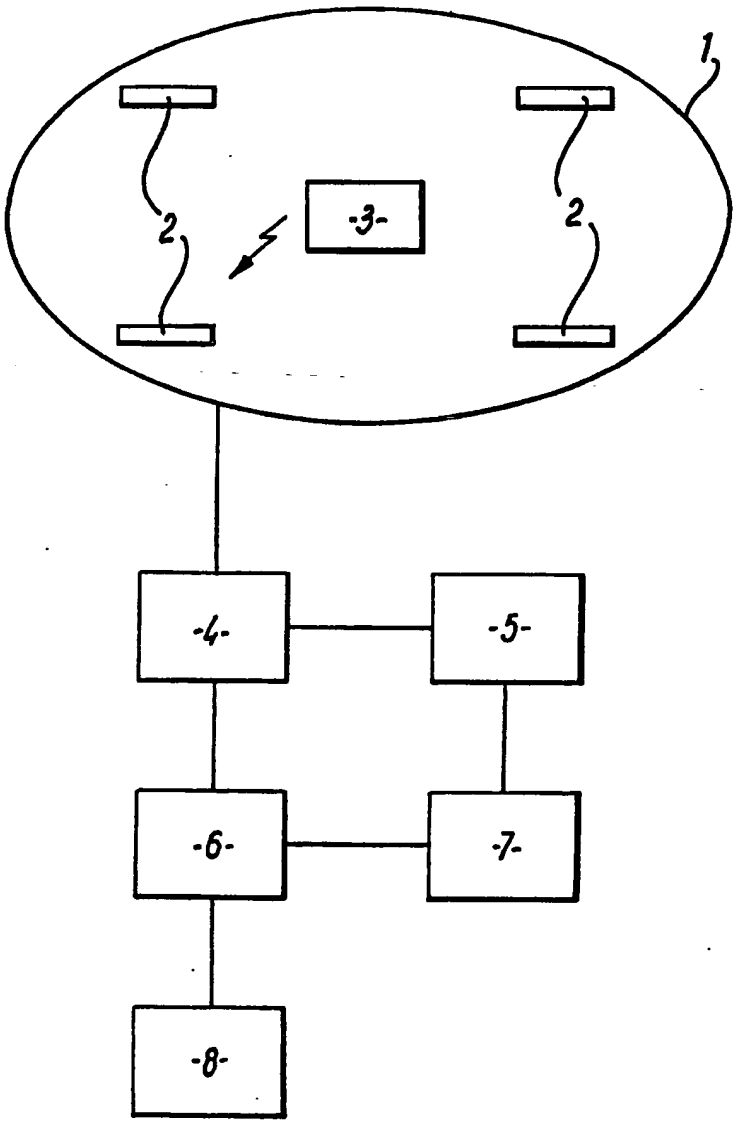

FIG.1

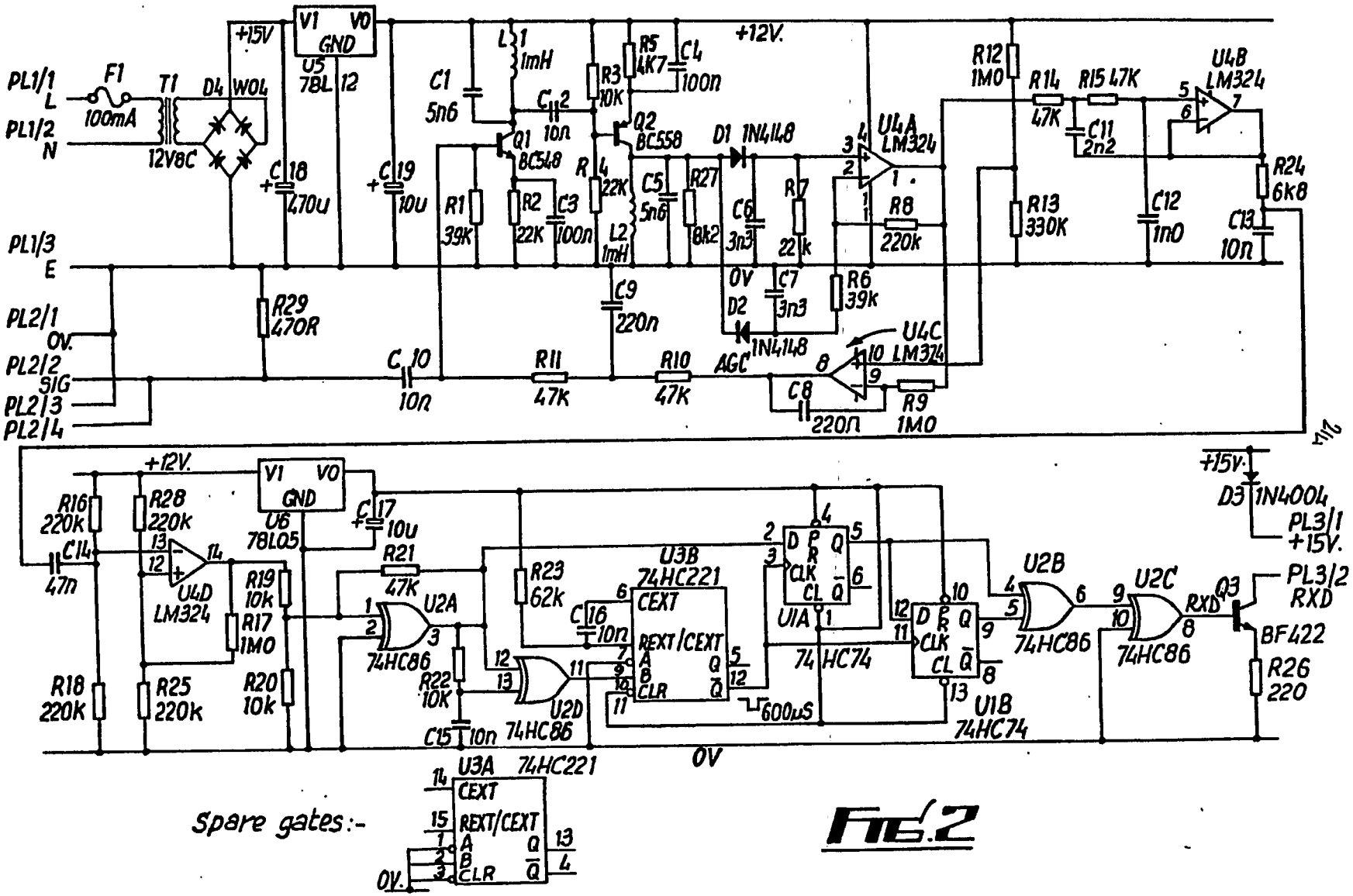
PL1/1 L
PL1/2 N
PL1/3 E
PL2/1 0V.
PL2/2 SIG
PL2/3
PL2/4
F1 100mA
T1
D4 W04
12V8C
+15V
V1 V0 GND
U5 78L12
C18 470u
C19 10u
C1 5n6
L1 1mH
C2 10n
R3 10K
R5 4K7
C4 100n
+12V.
Q1 BC548
Q2 BC558
D1 1N4148
R1 39K
R2 22K
C3 100n
R4 22K
L2 1mH
C5 5n6
R27 8k2
C6 3n3
R7 22k
U4A LM324
R8 220k
R12 1M0
R14 47K
R15 47K
C11 2n2
U4B LM324
R13 330K
C12 1n0
R24 6k8
C13 10n
R29 470R
C9 220n
0V
D2 1N4148
C7 3n3
R6 39k
U4C LM324
C8 220n
R9 1M0
C10 10n
R11 47k
R10 47k
AGC
+12V.
R16 220k
R28 220k
C14 47n
U4D LM324
R19 10k
R17 1M0
R18 220k
R25 220k
R20 10k
V1 V0 GND
U6 78L05
C17 10u
R21 47k
U2A 74HC86
R22 10K
C15 10n
R23 62k
U2D 74HC86
U3B 74HC221
C16 10n
CEXT
REXT/CEXT
A
B
CLR
Q
Q̄
600µS
U1A 74HC74
U1B 74HC74
U2B 74HC86
U2C 74HC86
Q3 BF422
R26 220
RXD
PL3/2 RXD
+15V.
D3 1N4004
PL3/1 +15V.
0V
U3A 74HC221
0V.
Spare gates:-

FIG.2

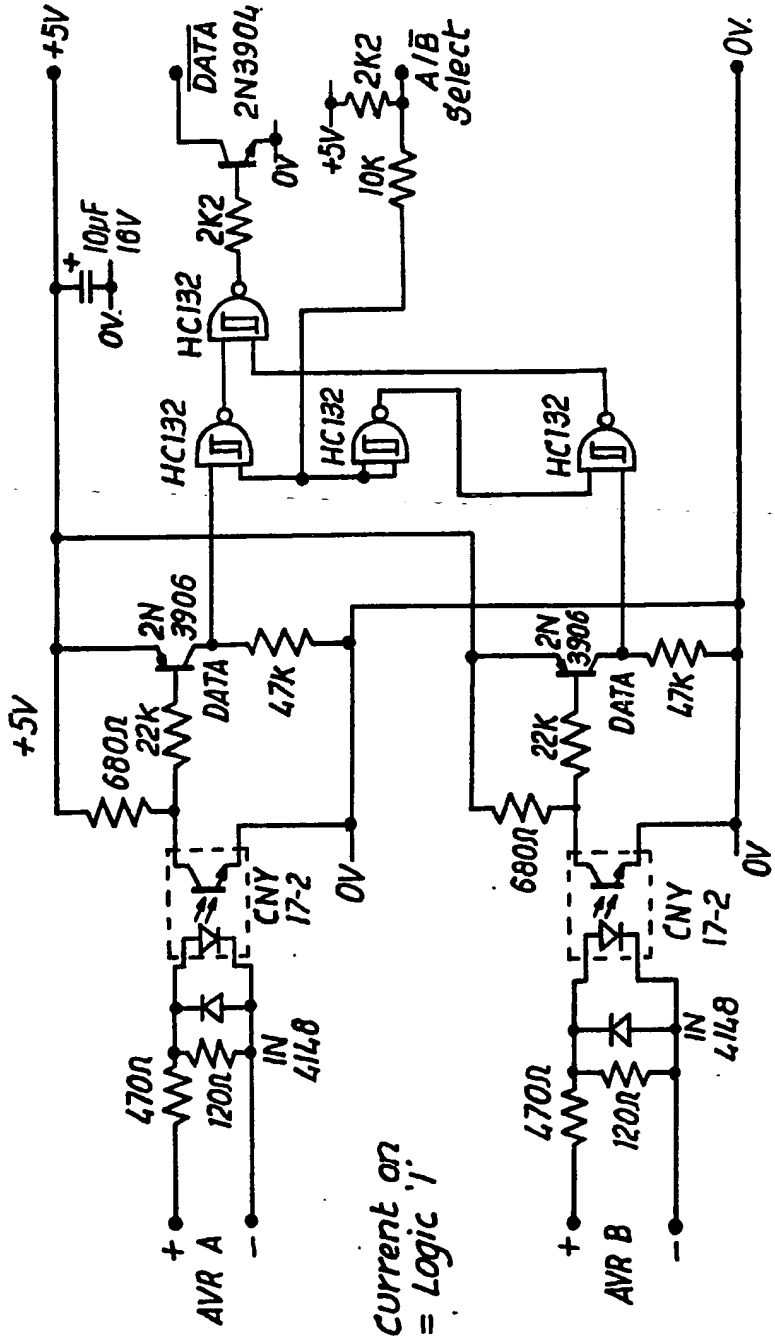
+5V
0V.
10µF 16V
DATA
2N3904
0V
2K2
+5V
10K
2K2
A/B select
HC132
HC132
HC132
HC132
2N 3906
DATA
47K
680Ω
22K
CNY 17-2
470Ω
120Ω
IN 4148
AVR A
AVR B
Current on = Logic '1'
0V

Fig. 3

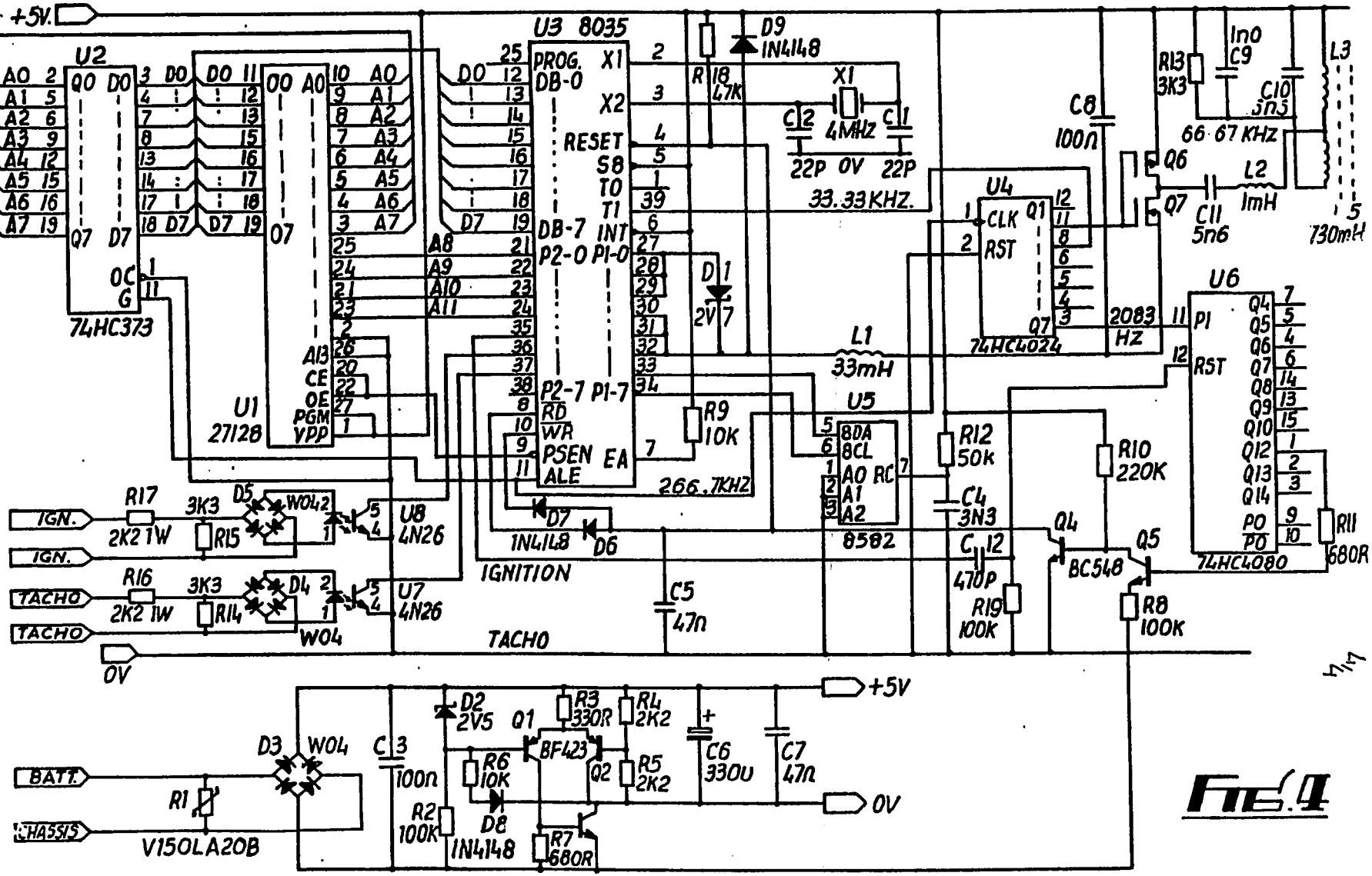
+5V.
U2
74HC373
U1
27128
U3 8035
PROG.
DB-0
RESET
SS
INT
PSEN
ALE
EA
RD
WR
X1
X2
T0
T1
P2-0
P1-0
P2-7
P1-7
DB-7
D9
IN4148
R18
47K
X1
4MHz
C2
C1
22P
0V
22P
33.33KHz.
C8
100n
U4
74HC4024
CLK
RST
Q1
Q7
2083
HZ
U6
74HC4080
P1
RST
L1
33mH
U5
8582
8DA
8CL
A0
A1
A2
RC
R9
10K
266.7KHz
D1
2V7
D7
IN4148
D6
IGNITION
C5
47n
TACHO
R12
50k
C4
3N3
C12
470P
R19
100K
R10
220K
Q4
BC548
Q5
R8
100K
R11
680R
R13
3K3
C9
In0
C10
3n3
66.67KHz
Q6
Q7
L2
1mH
C11
5n6
L3
730mH
IGN.
R17
3K3
2K2 1W
R15
D5
W04
U8
4N26
R16
3K3
2K2 1W
R14
D4
W04
U7
4N26
TACHO
0V
BATT.
CHASSIS
R1
V150LA20B
D3
W04
C3
100n
D2
2V5
Q1
BF423
Q2
R3
330R
R4
2K2
R5
2K2
R6
10K
R2
100K
D8
IN4148
R7
680R
C6
330U
C7
47n
+5V
0V

Fig.4

AUTOMATIC VEHICLE RECOGNITION SYSTEM AND DATA TRANSFER SYSTEM

The present invention relates to an automatic vehicle recognition system and data transfer system.

According to the invention there is provided an automatic vehicle recognition system comprising a transmitter for affixing to the vehicle a receiver for connecting to a vehicle station and means enabling the transmitter to be triggered when the vehicle reaches the station to send information to the receiver and means for manipulating the information.

In a preferred embodiment of the invention, a loop is embedded in the ground at the vehicle station. This is disposed to receive information transmitted by the vehicle transmitter. The loop is connected to the receiver and the receiver to a central computer for information processing.

The system may be powered up by means of an external switch, by switching the vehicle ignition off and by proximity, for example, when the

vehicle is inside the loop. Information relating to vehicle mileage, weight, fuel consumption and reserve, fleet number and depot number and other non-variable vehicle information may be transferred.

In order that the invention may be more clearly understood one embodiment thereof will now be described by way of example with reference to the accompanying drawings, in which:-

Figure 1 shows a block circuit diagram of a vehicle servicing station.

Figure 2 is a circuit diagram of a vehicle receiver,

Figure 3 is a circuit diagram of a vehicle recognition interface, and

Figure 4 is a circuit diagram of a vehicle transmitter.

Referring to Figure 1, the system includes a vehicle station which comprises a ground embedded loop 1 into which a vehicle represented by its four wheels 2 may be driven. The vehicle carries a transmitter 3 connected to receive information

regarding fuel consumption, mileage,vehicle identification, and any other relevant data derived from condition monitors disposed about the vehicle data. This transmitter is operative to transmit data received to a receiver disposed at the station. This receiver comprises a low Q RF front end tuning unit 4, a detection carrier remover 5, a square wave generator 6, an NRZ-F2F decoder 7 and a personal computer 8.

The circuit will now be described with reference to Figures 2,3 and 4.

Transmitter Hardware Description

This circuit description applies to circuit diagram 12875.

Operation.

The transmitter is designed to count tacho pulses and store them in non-volatile memory. When power is removed from the ignition input, the information stored in the memory is transmitted as F/2F modulation of a 67KHz carrier. Radiation is by a ferrite rod aerial which couples inductively to a ground loop.

Microprocessor

The microporcessor chosen is an 80C35 from

the 8048 family of Intel microcontrollers. It is a CMOS part as this gives reduced power dissipation in the voltage regulator pass transistor and a wide operating temperature range. It is also sourced by several manufacturers including Mullard, NEC and Intel.

The microprocessor runs at a low clock speed of 4MHz, chosen to give 67KHz (Carrier) when ALE is used to drive a simple divider.

Program Memory

The memory is a 27C64 or 27C128 EPROM (the parts are interchangeable in this design). CMOS parts are again chosen. U2 is a latch which multiplexes the data/address bus. It is possible to use a version of the 8035 with on-board EPPROM (8748) or use a masked microporcessor (8048) in which case the memory and latch integrated circuits should not be fitted.

Memory access time is not critical in this application because of the slow clock speed, and the slowest speed parts may be used.

Data Memory

The 8035 has 32 bytes of data memory on-chip which is used for the normal program operation,

storage of tacho pulses and the tens of kilometres count. The remaining kilometres information is stored in non-volatile memory in the form of a PCD8582. This component is an Electrically Eraseable PROM (EEPROM). Although it contains 256 bytes of storage, only just over 64 bytes is actually used. This means that alternative devices such as the PCD8572 from GE or the X2402I from XICOR may also be used. The alternative parts must be the wide temperature range parts, which are readily available. Communication with the memory is by a serial protocol. Briefly, communication is over a 2-wire bus (clock and data) started with a device address from the master (the 8035 in this case) and controlled by acknowledges from the device receiving data. Three blocks of data are stored in the non-volatile memory; the vehicle ID, the tacho calibration (pulses per kilometre) and the current tach reading (up to 6 digits) excluding tens of kilometres. Data is stored in blocks of four bytes; three bytes of data and a checksum. Each memory location may be written to 10,000 times. The software design means that each tacho location is written to every 160 kilometres, giving a memory life of 1,600,000 kilometrs. The data storage allows a maximum figure of 9,999,990 kilometres to be stored. Both of these figures

should exceed the requirements.

Loss of power will cause loss of the tens of kilometres reading and the tacho pulse count; this should be a rare event however, as in normal operation the power is never removed.

Watchdog timer

ALE is divided down by U4 and then U6 to give a reset pulse on pin 3 of U6 approximately every 8 seconds. In normal operation, the microprocessor will output negative (watch dog) pulses periodically which will couple through C12 to the reset pin on U6. This will normally prevent U6 applying a reset to the microprocessor. The microprocessor output is coupled capacitively to the counter reset input so that a reset is caused by an active transition on the processor output rather than a level.

Reset

The microprocessor is held in reset by Q4 until the input voltage to the voltage regulator exceeds approximately 8V. At this level the current drawn through R8 is more than the current supplied by R10. Q4 therefore turns off, releasing the reset input.

If the watchdog timer should time out, then the Q14 output of U6 will go high, forcing Q4 on by forward biasing the collector-base junction of Q5.

If a read or write to external data memory is attempted, then D6 or D7 will conduct, discharging C5 and also causing a reset.

Carrier generation and modulation.

The carrier is generated by taking the Q2 output of U4, giving a carrier frequency of 66.667kHz. This is applied to the push-pull fet pair Q6 and Q7. The power for this pair of transistors is provided by microprocessor outputs switching to ground. These outputs are arranged in triples to obtain sufficient current sinking ability. One triple switches directly to ground, causing the full 5V rail to be applied to Q6 and Q7. The other triple switches to ground via a zener diode which drops some of the supply voltage so that a reduced supply voltage is applied to Q6 and Q7. When both triples are off (high) no voltage is applied to Q6 and Q7 and the transmitter is turned off.

The modulation is therefore Amplitude modulation switching between two possible

amplitudes. The data to be transmitted is NRZ (RS232) data, but before transmission, it is converted to F/2F coding. This method of encoding involves a level change at the start of each bit cell, and an additional level change in the middle of the bit cell if the bit being transmitted is a zero. The reason for choosing this method of modulation is that the amplitude is caused to change frequently regardless of the data pattern being transmitted. The average received carrier level is therefore independent of the data pattern and the AGC circuit in the receiver does not attempt to track long term changes in signal level caused by varying data patterns. This in turn reduces the amount of 'skew' on the received data signal, improving the quality.

The signal at the drains of Q6 and Q7 is a square wave (rich in odd harmonics), so a series resonant circuit is chosen to pass the signal on to the transmitting coil. A Q-factor of 10 is chosen to pass the signal onto the transmitting coil. A Q-factor of 10 is chosen for this circuit, so that a resonable sinewave is obtained without requiring tuning of individual components. (A Q-factor of 10 can be achieved with 5% components without having to trim the component values further). This signal is then applied to

the tuned ferrite rod aerial which further improves the wave shape. The loading on this circuit and thus the series resonant circuit is determined by R13 and the metal transmitter plate. The load must be fairly well defined as it in turn determines the load that Q6 and Q7 present to the low pass filter components L1 and C8. A Q-factor of 10 is again aimed for to avoid the need to adjust individual component values. C9 is provided if a trim proves to be necessary.

Filter components L1 and C8 limit the rate of change of amplitude of the carrier and therefore control the bandwidth occupied by the carrier. They are chosen to pass the maximum modulating frequency of 1200Hz (when transmitting a string of zeroes) but to start attenuating at the second harmonic of 1200Hz and above. The filter performance is determined by the load presented by Q6 and Q7 and therefore the load presented by the aerial. If the loading is too small, then the modulating signal will tend to overshoot and 'ring'; if the loading is too great the modulating signal will change too slowly and will distort the data pattern being transmitted.

D9 prevent damage to the microprocessor outputs due to inductive discharge from L1 when

the transmitter turns off.

Voltage regulator

The voltage regulator is a discrete component design, since it must withstand considerable over-voltage transients applied to the input. It is a conventional series-pass design with a reference which is powered mainly from the output once the regulator has started. R2 and D8 ensure that the regulator starts-up. A negative regulator is chosen because high voltage, moderate-power NPN transistors are cheaper than the equivalent PNP transistors. The pass transistor power dissipation is small, even when running from a +24V input because the microprocessor and memory are both CMOS parts. The voltage regulator is preceded by a diode bridge, so polarity is unimportant and the nomination of battery and chassis inputs is arbitrary. R1 gives protection against short voltage transients, such as ignition noise.

Inputs

Both the Tacho and Ignition inputs are by bridge rectifier and opto-coupler. This gives great flexibility in the type and connection (relative to chassis) of each input. Vehicle earth (positive or negative) is unimportant. The inputs

are also highly immune to damage (e.g. application of excessive or reverse voltages).

TRANSMITTER SOFTWARE DESCRIPTION (Figure 4)

The software can be in one of three different states:-

1. Ignition on state,
2. Transmit state,
3. Calibrate state.

Each state is described below.

Ignition On State (IGNON)

The software will enter this state when the ignition optocoupler has power applied to it. In this condition the software will wait for pulses to appear on the tacho input and count them. Each pulse will produce a call to TACHO. This reads in the number of pulses per kilometre (TACHOCAL) from the non-volatile memory and compares it with the incremented total in ram (CNT2,CNT1, CNTO).. TACHOCAL is stored in non-volatile memory as a three byte packed BCD number plus one check byte. If the check fails then a default value of TACHOCAL (DEF2,DEF1,DEFO) is used, otherise a default of 0 would be used which would cause the tacho count to become very inaccurate very fast.

If the pulse count is equal to TACHOCAL then

the kilometres count in ram (KMS) is incremented by 1. If this count reaches 10 then it is reset to 0 and the non-volatile memory is read for the highest value of valid tacho reading. This count is then increased by 1 and stored in the next non-volatile memory location.

The maximum stored tacho reading is found by calling TACHORDG. This scans 16 blocks each of 4 bytes of non-volatile memory and checks each one for valid data. The check is made by recalculating the check byte from the 3 data bytes and comparing it with the stored check byte. If they are equal, then the new data is accepted, otehrwise the data is cleared to all zeroes. This process is repeated on all 16 blocks, storing the maximum value so far found in ram (TMAX), so that at the end, the value in TMAX is the largest tacho reading found. This value, which is in packed BCD form, is incremented by 1 and stored in the next block with block 16 wrapping around onto block 0. This system ensures that if corruption of the last tacho reading should occur (for example if power was removed during the write of the last update) then the next highest count is used, which will be only 1 count less. This sytem is used only to store the tacho reading because this is the only value which is constantly being re-written to the

non-volatile memory.

Transmit On State (TRANSMIT)

This is the state entered on reset or when power is removed from the ignition optocoupler.

The transmitter is turned on, and data from non-volatile memory is read into ram prior to transmission. The data is read in the following sequence, and checked for validity, non-valid blocks being replaced with OOH,OOH,OOH:-

Three blocks of vehicle ID (9 bytes of ascii data in total)

The tacho calibration figure (3 bytes of packed BCD)

The highest tacho reading (3 bytes of packed BCD)

The kilometres digit is then fetched from RAM and appended to the 6 digits fetched from NVRAM. A dummy zero is also added after the kilometres digit - this should be ignored. This data is then transmitted after a pre-amble of F/2F encoded '1' to synchronise the receiver F/2F-to-NRZ decoder. Note that the vehicle ID data is transmitted

byte-for-byte whereas the packed BCD data is unpacked and converted to ascii before transmission. The data is preceded by the characters <23 and is terminted by > followed by a longitudinal redundancy check byte and a checksum byte. Neither check byte takes account of data following the > character.

The longitudinal check byte is formed by forming the exclusive-or function of all the transmitted characters upto and including the> character.

The checksum byte is formed by subtracting all the characters from 0, upto and including the > character.

The transmission is repeated 255 times, so that the total transmission lasts for about 90 seconds.

The data transmitted is 1200 baud, 7-bit data, odd parity and two stop bits. Timing is controlled by an interrupt routine CNTINT which interrupts every half-bit. It complements the F1 flag which is then used to decide whether the interrupt was at the start of a bit cell or halfway through it. A polling routine called WAIT

decides what to do after each interrupt.

The transmit state cannot be interrupted until complete. It finishes by moving to the Calibrate State.

Calibrate State (CALIB)

This state is entered from the completion of the transmit state and is left if the ignition optocoupler should turn on. It monitors the tacho optocoupler which in this state is used to send new calibration to the transmitter. It continually waits for a start bit transition and monitors and ignition optocoupler (RECSTRT).

Calibration data is sent as 9 vehicle ID bytes followed by 6 decimal tacho calibration bytes (in ascii form) followed by a longitudinal redundancy check byte and a checksum byte. These check bytes are formed in the same way as the transmitted data check bytes, and exclude themselves from the calculation.

The data received must be 1200 baud, 7-bit data, odd parity and one or two stop bits. If either check byte fails then the new data is discarded. If it is correct, then it is written to the non-volatile memory and all 16 tacho reading

blocks are reset to zero.

The transmit state is then re-entered so that the new data can be transmitted and checked. If either check byte failed then the old, unmodified, data will be transmitted.

Points regarding the 8048

The 8048 instruction set does not allow conditional jumps to occur across page (256 byte) program boundaries. This cannot be avoided in advance since the relative position of code and page boundaries is not known until after assembling and linking the code. The Avocet assembler will normally produce a language error at this point. It is then necessary to look at the avr.prn file to find out which line caused the problem and to insert NOP codes to push the problem jump 'over' the boundary. It should be noted that a line which jumps to itself will be missed as a language error if it lies on the page boundary. It will certainly not run correctly. The easiest way to ensure that there are no problems is to have a NOP instruction on all page boundaries (which can be tedious) or to use the Avocet simultator to try suspected problem areas and check them for correct operation.

Since there are only eight registers, only two of which may be used to point to the ram area, it is important to ensure that subroutines do not corrupt registers used by the calling routine. There is no instruction that allows data to be saved temporarily on the stack, other than FO,C and AC. An alternate register set is available, but this is only used by the timer interrupt (CNTINT) and only uses one alternate register. It's main use is in the debug routine DEBUG which can then be called anywhere in the program to output ram data as a transmitted string for debugging purposes, without corrupting registers in the process.

RECEIVER HARDWARE DESCRIPTION (Figure 2)

Power Supply

The receiver power supply is mains derived and is a simple transformer and bridge rectifier giving +12V after regulation to power and analogue section and +5V after regulation to power the digital section.

Receiver front-end

The reciver front-end is formed by Q1 and Q2. Q1 is a tuned load common emitter amplifier with gain control achieved by controlling the

transconductance through the bias current. The collector load at resonance is about 5 kohm formed by Q2 input impedance and bias network. This gives a maximum stage gain with no agc applied of about 20. The Q-factor is kept low to allow the use of standard components without any trimming. The pickup loop is tuned by a capacitor which may be connected between PL2 pins 3 and 4. A fixed capacitor may not be used here as the loop inductance will vary fron one site to the next. The loop Q is controlled by R29 which limits it to about 10.

Q2 is a tuned collector common emitter amplifer with a fixed gain of approximately 120. The collector load at resonance is about 3 kohm giving a Q-factor of about 7. This again allows the use of standard components without trimming. The collector load is produced by R27 and the two peak-rectifier diodes and loads which dissipate the same power as a single 5 kohm resistor straight across the coil would. (This then gives the equivalent load resistance from which the Q-factor may be calculated).

The total gain before agc is therefore about 2,400. The agc should begin to operate for input signals greater than about 200uV; the first stage

should not overload until about 20mV input giving an agc range of about 40dB.

Data reception should start at about 150uV input level. Assuming a 14kHz bandwidth and a source impedance not exceeding 470 ohms, the effective input noise should be less than 1uV giving a signal to noise ratio of 46dB at the onset of agc. This will be improved by a factor of about 5dB by filtering after the detector stage.

Detector and AGC

The detector is a full wave rectifier design using D1 and D2 to conduct on alternate half cycles. The loading on each diode is the same, but to achieve this, R6 is twice the value of R7 because it will have twice the voltage across it. (It will have the peak-to-peak voltage rather than peak-to ground voltage across it). C6 and C7 give some initial smoothing and U4 sums the two signals to give an output which is 12x (peak voltage less one diode drop). When this voltage reaches 3V, the agc integrator will start to discharge, reducing the current in the first stage which in turn reduces the first stage gain. C9 removes any modulation information from the agc line.

Filtering

The detected signal is filtered by a three pole filter (U4B) having a roll-off frequency of 2.4kHz. This is formed by a two-pole Butterworth design with an additional pole added on the output to increase the damping and improve the filtering. (Butterworth filters are slightly underdamped and therefore not ideal for digital data).

The filtered signal is capacitively coupled into a Schmitt trigger circuit (U4D). This circuit has an offset of 6V applied to both inputs and positive feedback of +/- 500mV applied added to the non-inverting input depending on the state of the ouptut. A minimum voltage swing of 1V is therefore needed to cause the output to change state.

NRZ Data Recovery

The output from U4D is fed into another (digital) Schmitt trigger to increase the edge speeds to digital speeds and to level shift at the same time to 5V.

Each edge is then fed to U2D directly and via R22 and C15 to produce a short positive pulse at the monostable input on every edge (positive or negative). The monostable is non-retriggerable

with a period of 3/4 of a bit cell. It therefore synchronises to the start of each bit cell (which always has a transition) rather than the middle of the bit cell (which only has a transitin of a '0' is being transmitted). This recovered clock signal is used to shift data into U1A and then U1B. An exclusive or gate then compares successive data state at the beginning of each bit cell. If the data level is the same at the start of two successive bit cells, then there must have been two intervening transitions and therefore the data bit was a '0'. Otherwise there data compared is different and there was only one intervening transition (the start of the next bit cell) and the data was therefore a '1'.

Data is output by Q3 which is configured as a constant current drive circuit. A received '1' is represented by the constant current being turned on, and a received '0' is represented by no output current.

Q3 is a high voltage device to give it a degree of protection, and D3 protects the power supply from excessive external (positive) voltages. The output is designed to be terminated by an optocoupler at the distant end.

It will be appreciated that the above embodiment has been described by way of example only and that many variations are possible without departing from the invention.

CLAIMS

1. An automatic vehicle recognition system comprising a transmitter for affixing to the vehicle a receiver for connecting to a vehicle station and means enabling the transmitter to be triggered when the vehicle reaches the station to send information to the receiver and means for manipulating the information.

2. An automatic vehicle recognition system as claimed in claim 1, comprising a loop adapted to be embedded in the ground at the vehicle station and disposed to receive information transmitted by the vehicle transmitter.

3. An automatic vehicle recognition system as claimed in claim 2, in which the loop is connected to the receiver and the receiver to a central computer for information processing.

4. An automatic vehicle recognition system as claimed in claim 1,2 or 3, in which the system is arranged to be powered up by means of an external switch.

5. An automatic vehicle recognition system as claimed in claim 4, in which the switch is the ignition switch of the vehicle.

6. An automatic vehicle recognition system as claimed in any preceding claim, in which the receiver is operative to receive information regarding fuel consumption, mileage and vehicle identification.

7. An automatic vehicle recognition system as claimed in any preceding claim, in which the receiver comprises a low Q RF front end tuning unit, a detection carrier remover, a square-wave generator, a decoder and a computer.

8. An automatic vehicle recognition system as claimed in any preceding claim, in which the transmitter is operative to count tacho pulses and store them in a non-volatile memory.

9. An automatic vehicle recognition system as claimed in claim 2, in which an aerial is connected to the loop.

10. An automatic vehicle recognition system substantially as hereinbefore described with reference to the accompanying drawings.

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